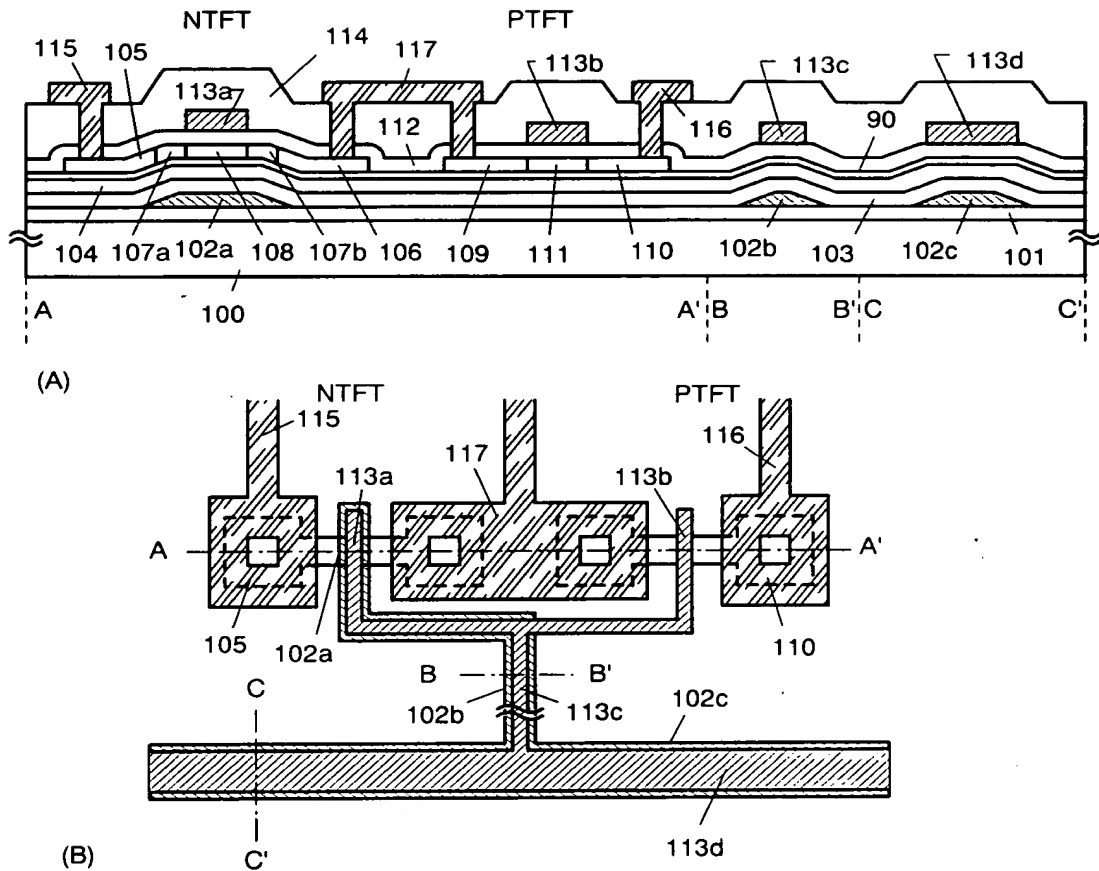


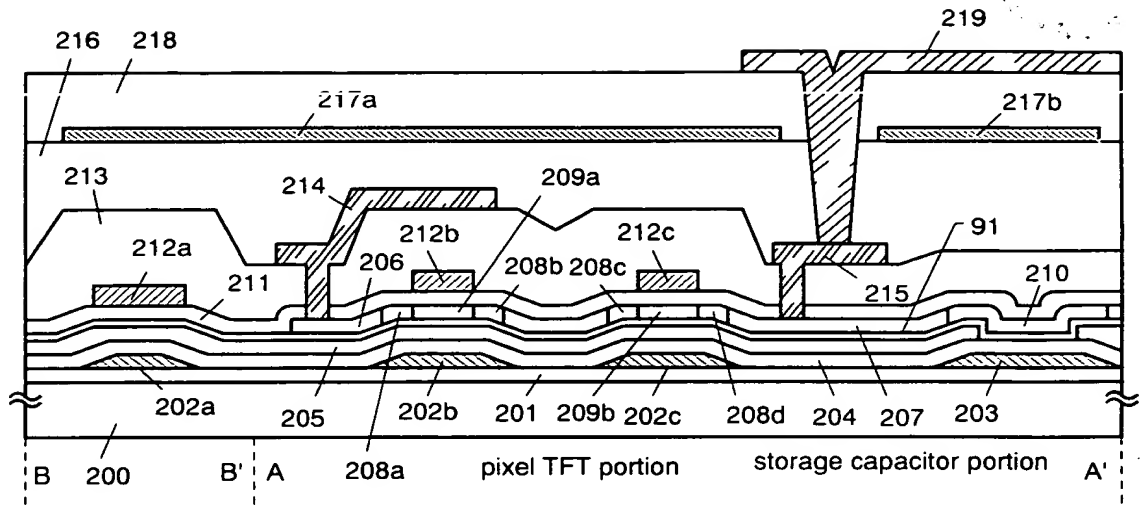
[Name of Document] Drawing

[Fig. 1]

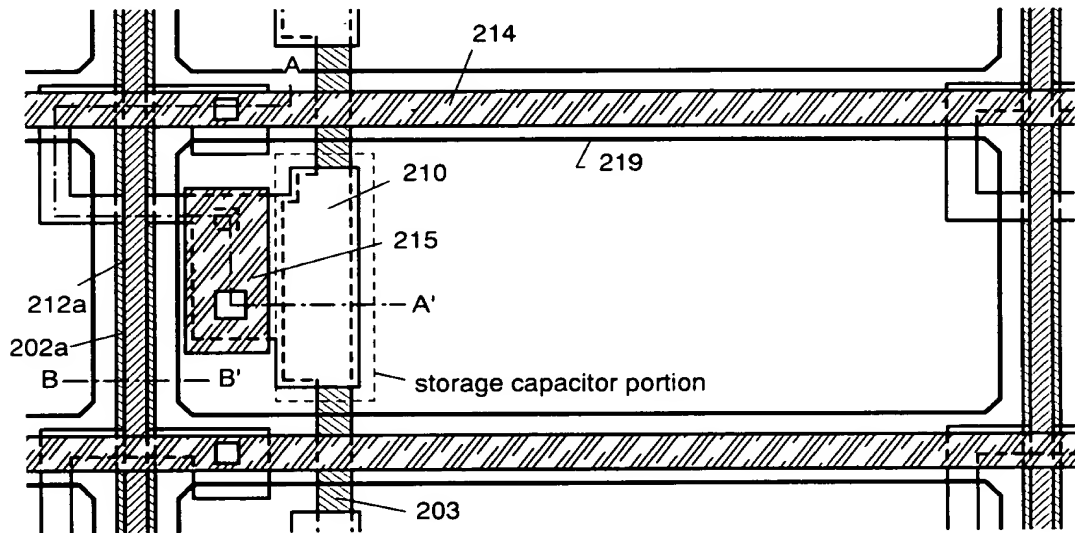


100: substrate 101: base film 102a, 102b, 102c: first wiring lines 103: first insulating layer  
 104: second insulating layer 105: source region (NTFT) 106: drain region (NTFT)  
 107a, 107b: low concentration impurity region 108: channel formation region  
 109: source region (PTFT) 110: drain region (PTFT) 111: channel formation region (PTFT)  
 112: second insulating layer 113a, 113b, 113c, 113d: second wiring lines  
 114: first interlayer insulating layer 115: source wiring line (NTFT)  
 116: source wiring line (PTFT) 117: drain wiring line (in common with NTFT and PTFT)

[Fig. 2]



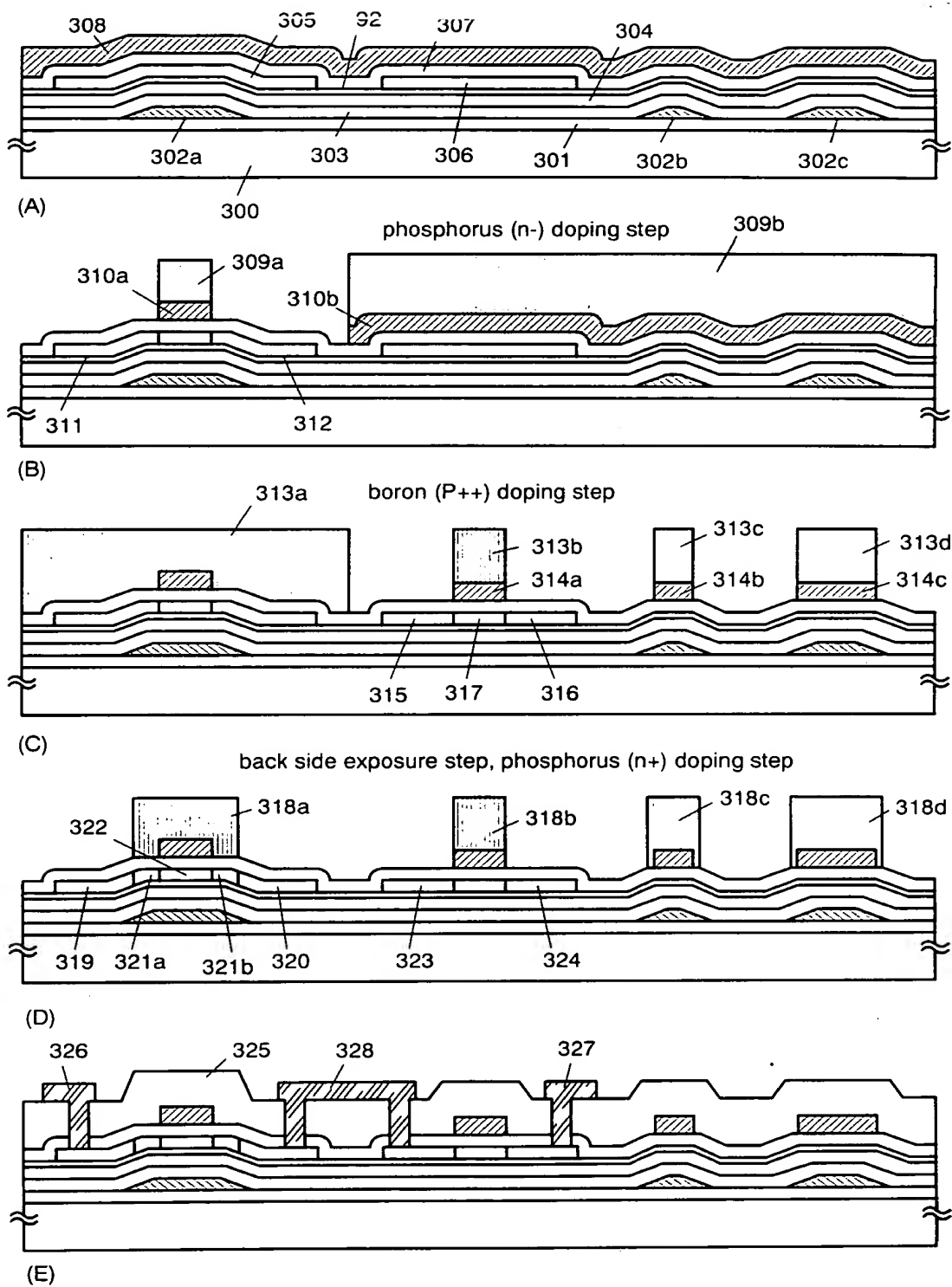
(A)



(B)

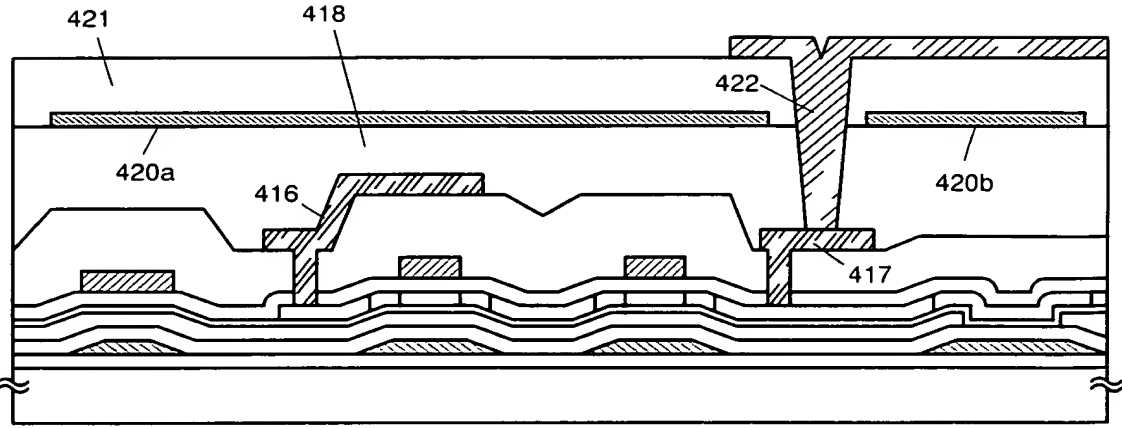
200: substrate 201: base film 202a, 202b, 202c: first wiring lines 203: capacitor wiring line  
 204: first insulating layer (TaOx film) 205: second insulating layer 90: silicon oxide film  
 206: source region 207: drain region 208a to 208d: low concentration impurity region  
 209a, 209b: channel formation region 210: impurity region for a capacitor  
 211: third insulating layer 212a, 212b, 212c: second wiring lines  
 213: first interlayer insulating layer 214: source wiring line 215: drain wiring line  
 216: second interlayer insulating layer 217a, 217b: black mask  
 218: third interlayer insulating layer 219: pixel electrode

[Fig. 3]

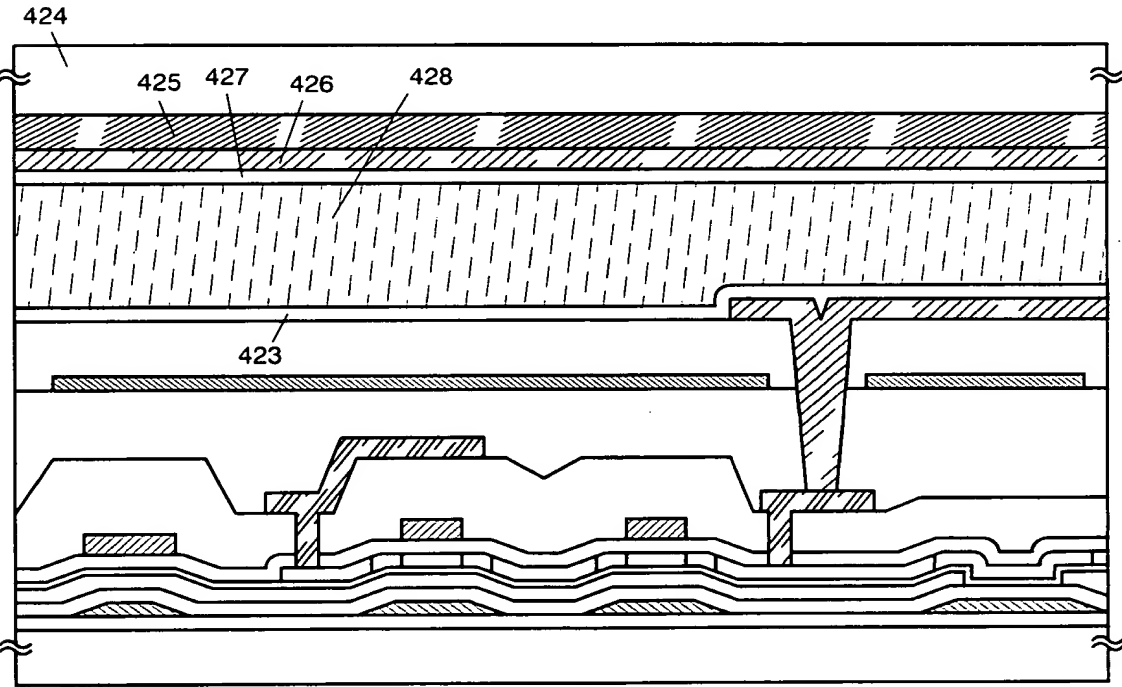




[Fig. 5]

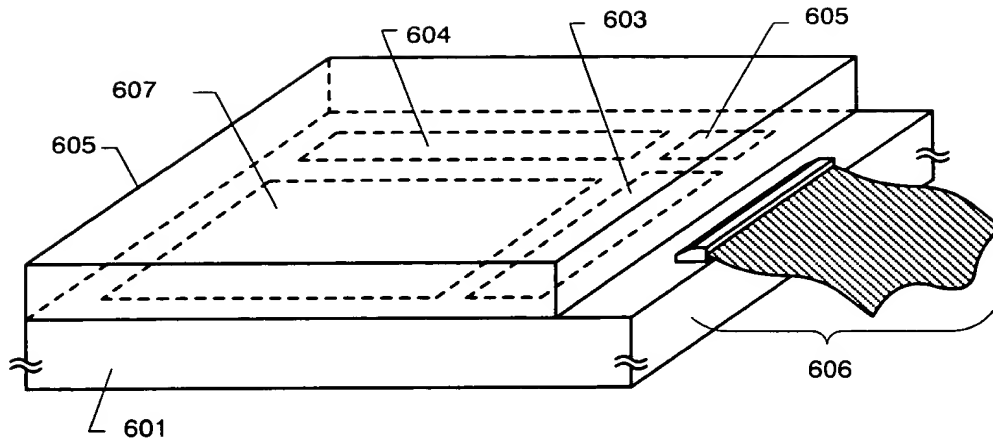


(A)



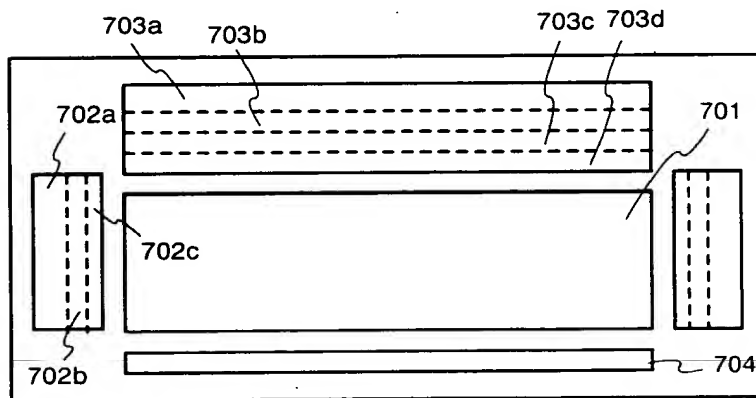
(B)

[Fig. 6]



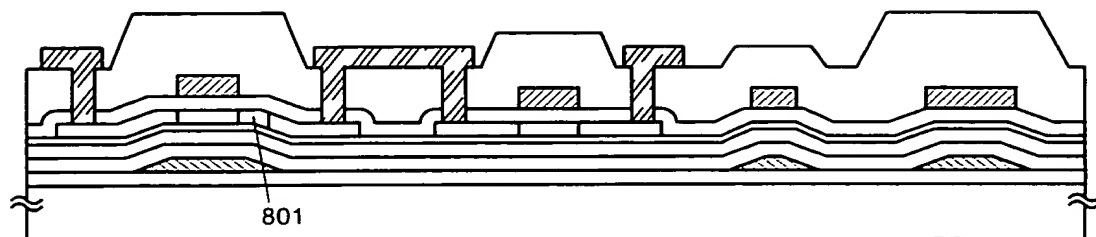
601: substrate with an insulating surface 602: pixel matrix substrate  
 603: source driver circuit 604: gate driver circuit  
 605: signal processing circuit 606: FPC 607: opposite substrate

[Fig. 7]

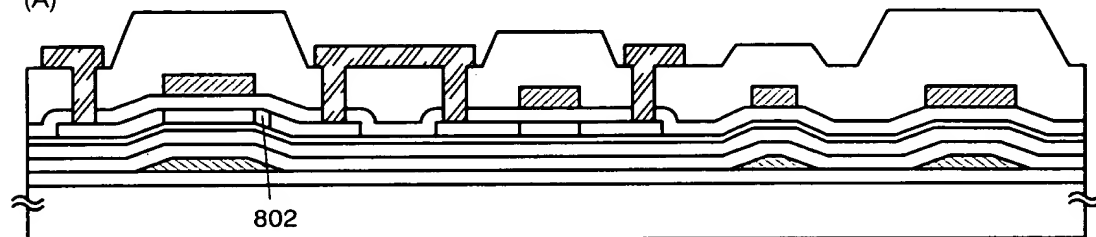


701: pixel matrix circuit 702a, 703a: shift register circuit  
 702b 703b: level shifter circuit 702c, 703c: buffer circuit  
 703d: sampling circuit 704: precharge circuit

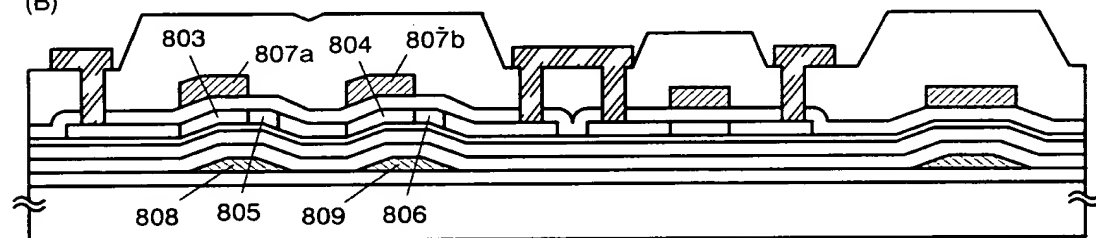
[Fig. 8]



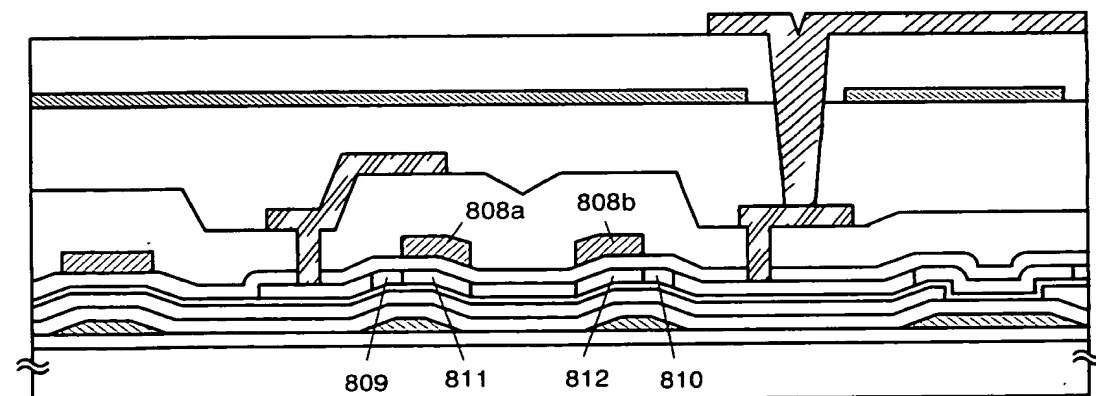
(A)



(B)

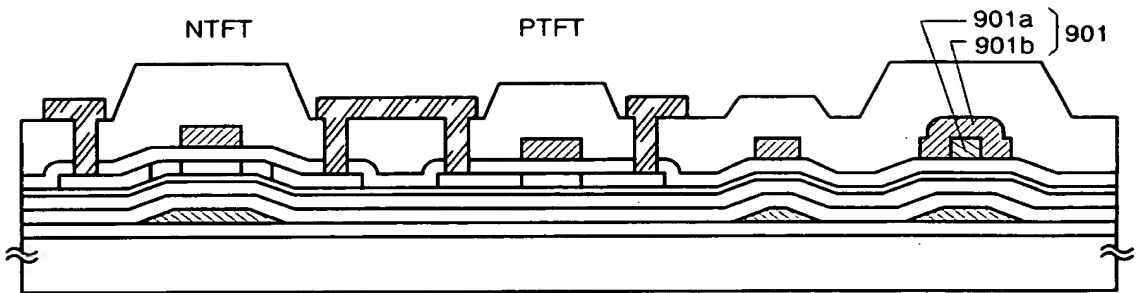


(C)

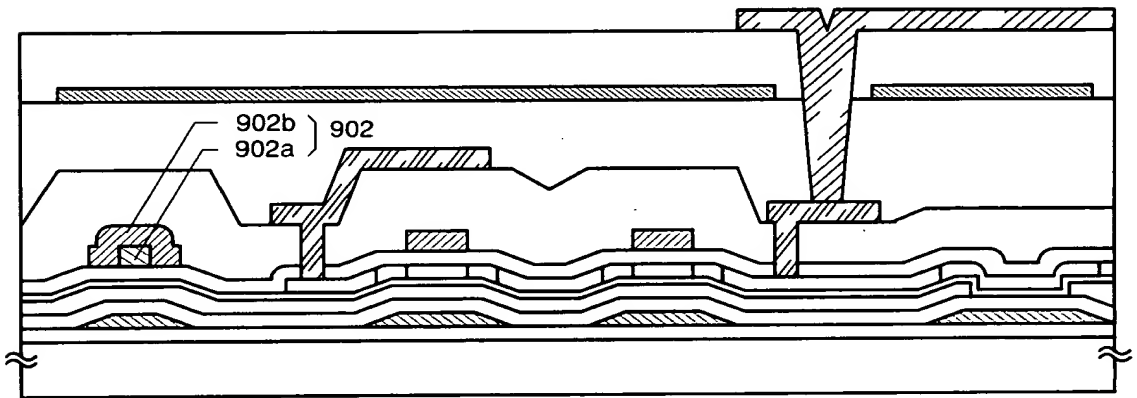


(D)

[Fig. 9]



(A)

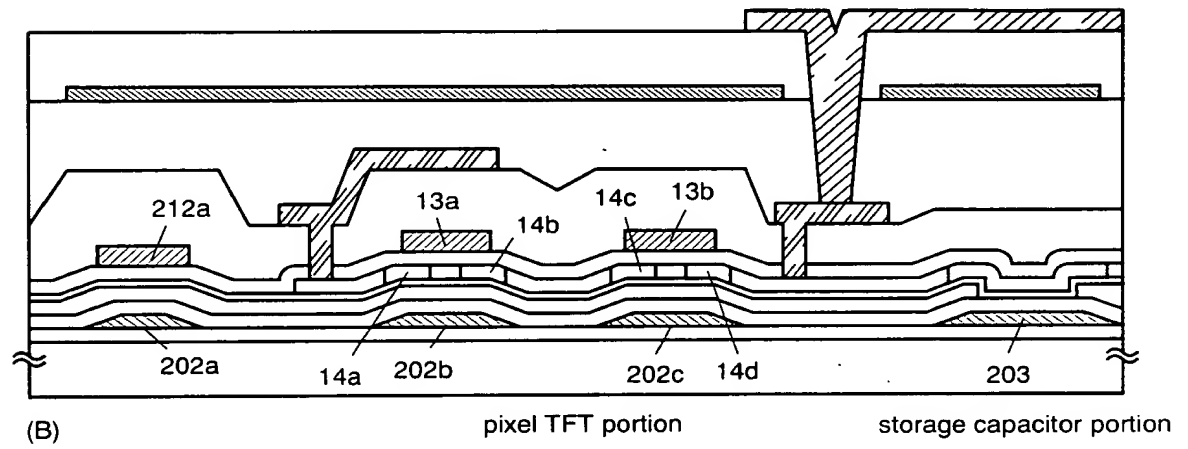
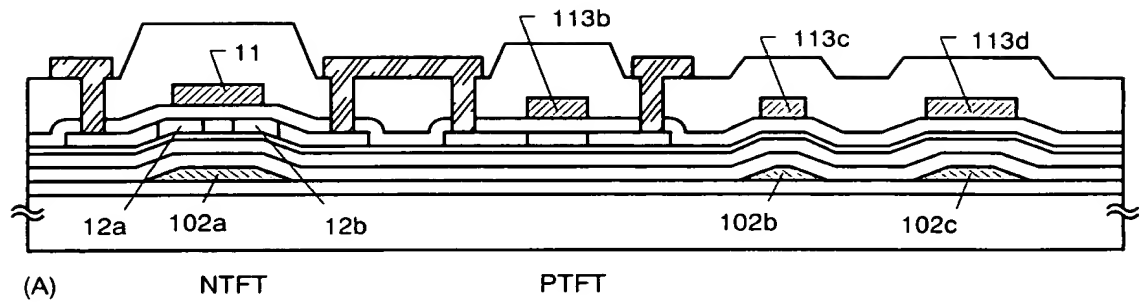


(B)

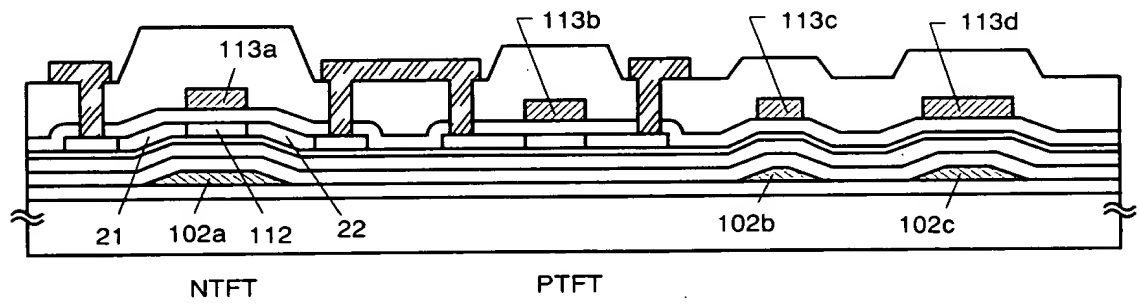
pixel TFT portion

storage capacitor portion

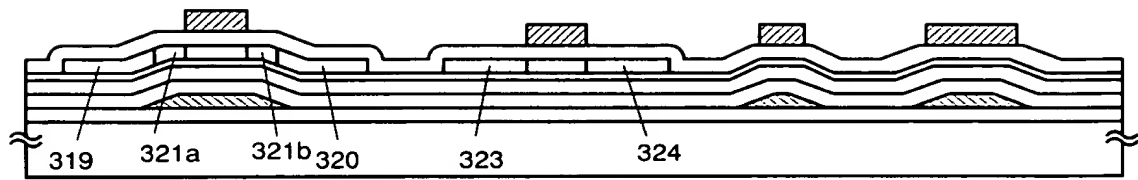
[Fig. 10]



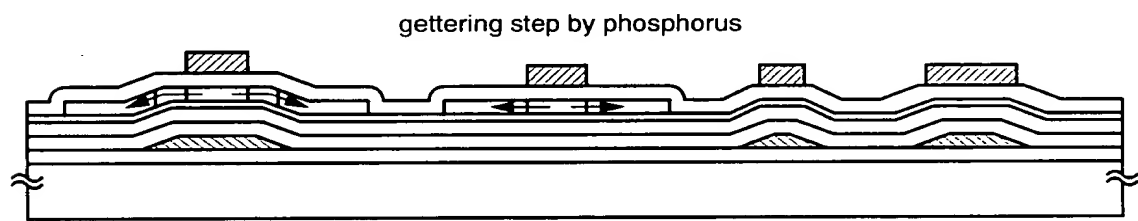
[Fig. 11]



[Fig. 12]

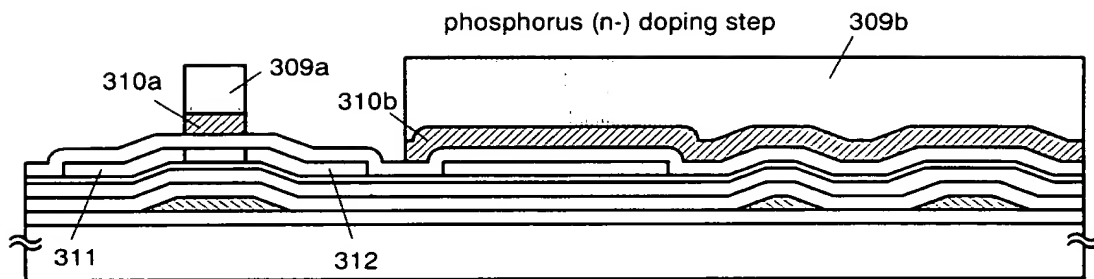


(A)

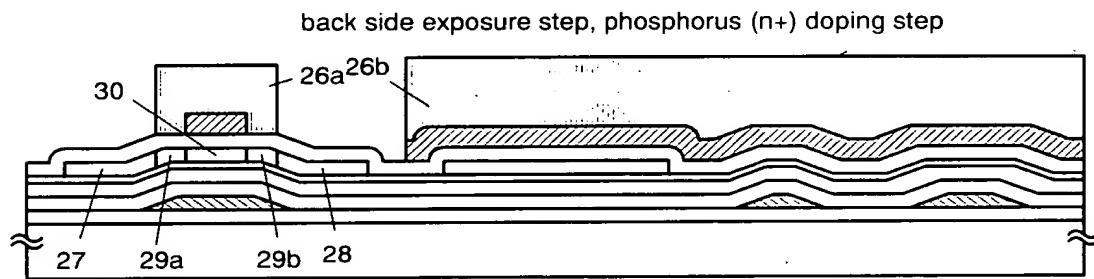


(B)

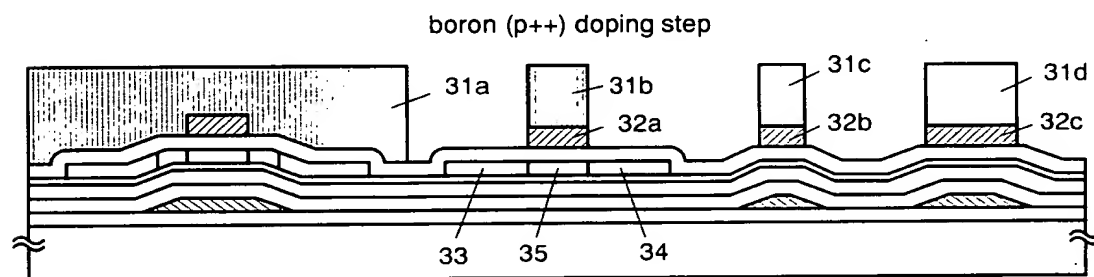
[Fig. 13]



(A)

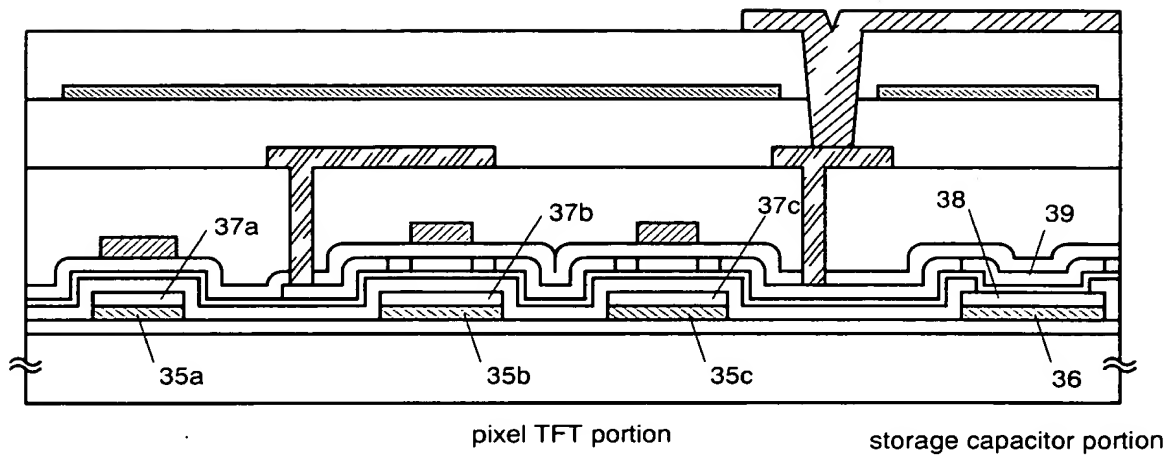


(B)

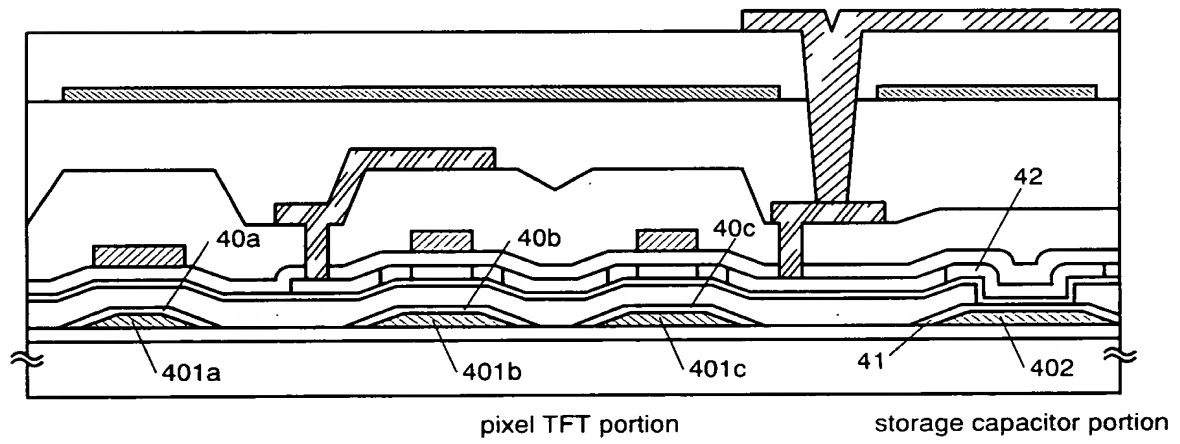


(C)

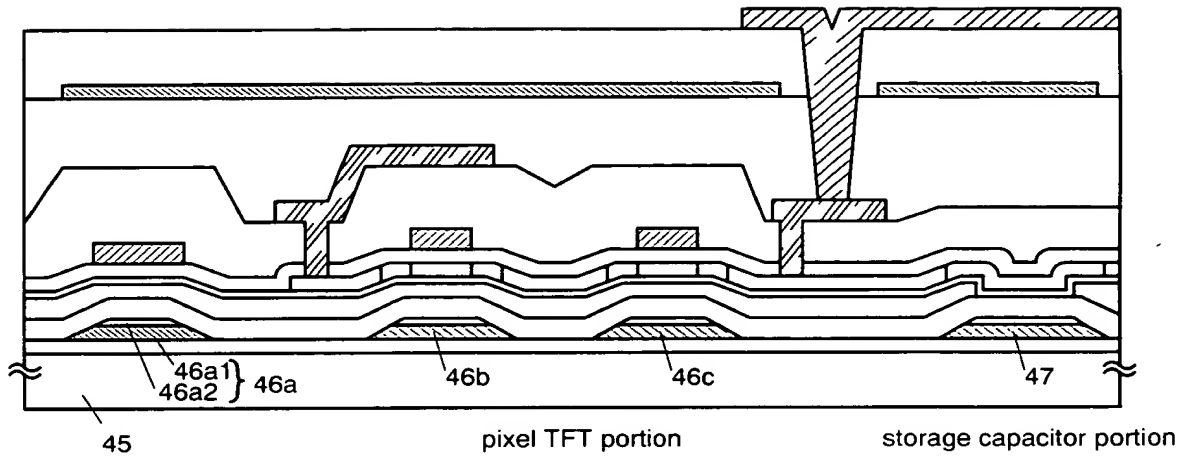
[Fig. 14]



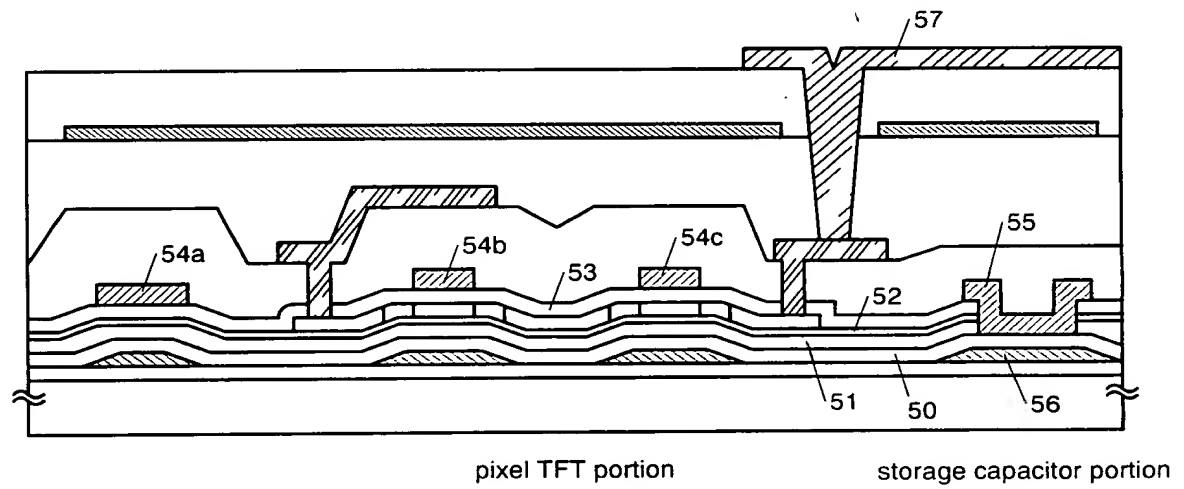
[Fig. 15]



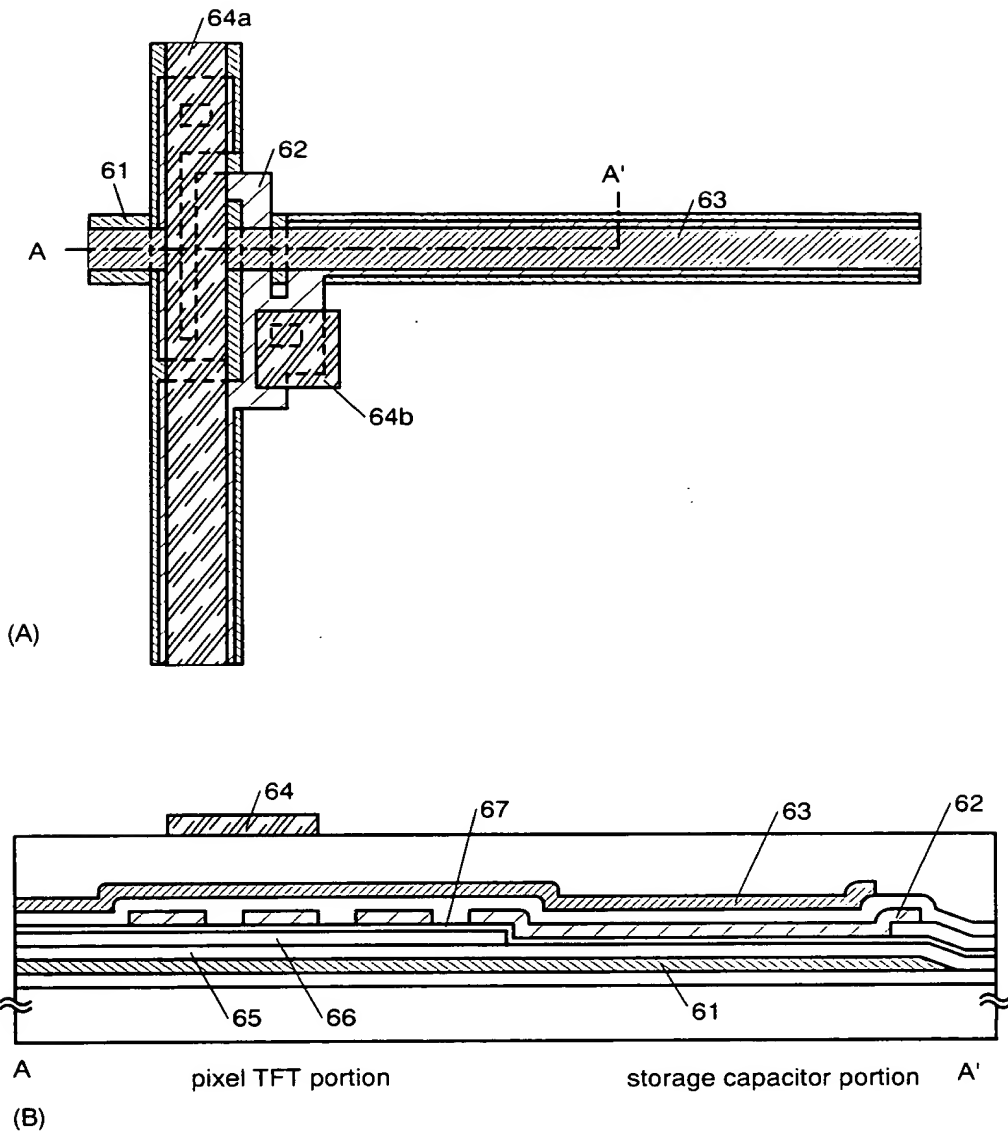
[Fig. 16]



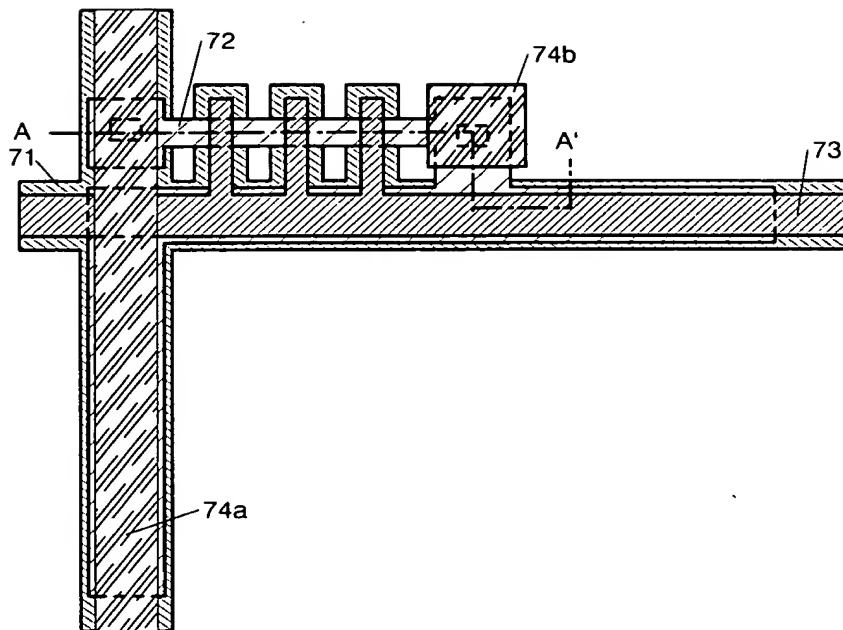
[Fig. 17]



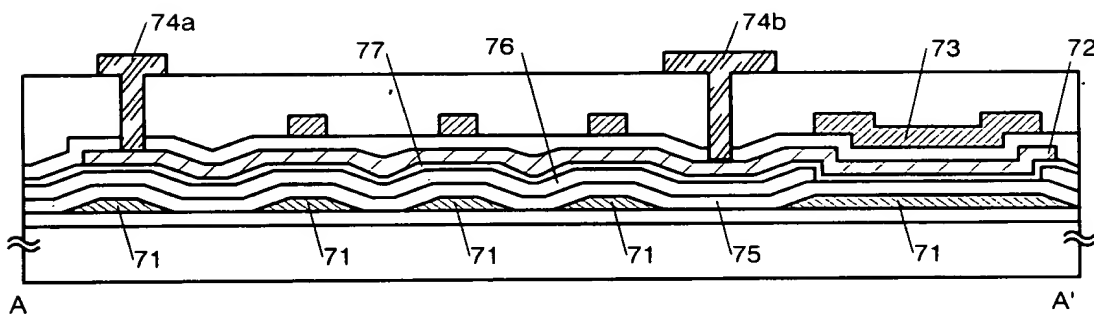
[Fig. 18]



[Fig. 19]



(A)

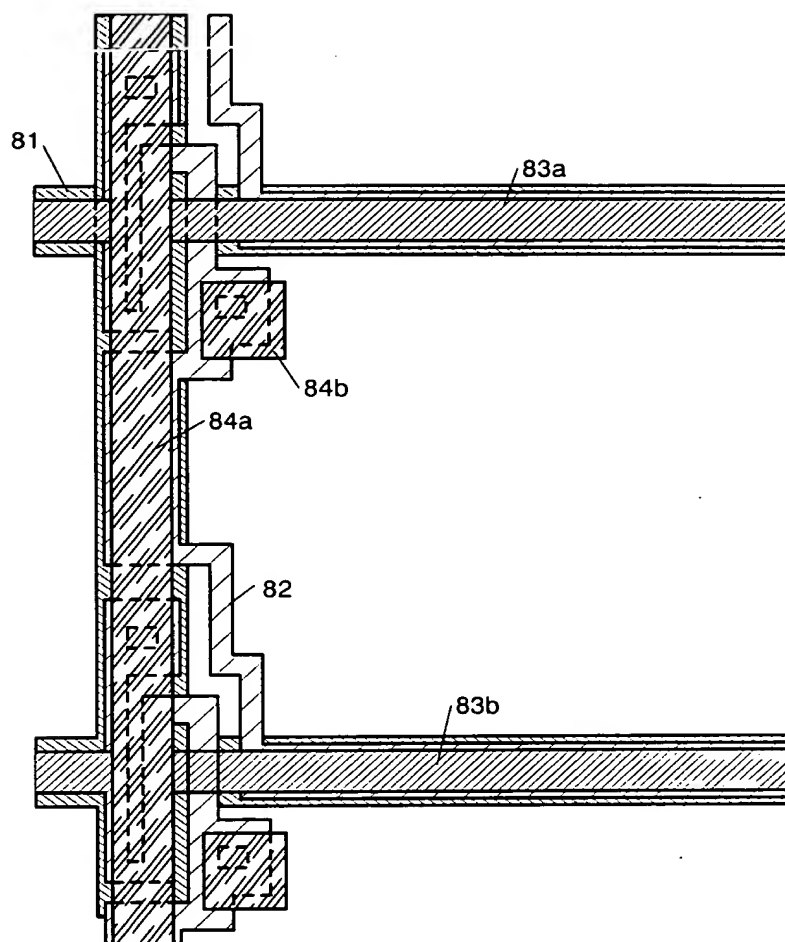


(B)

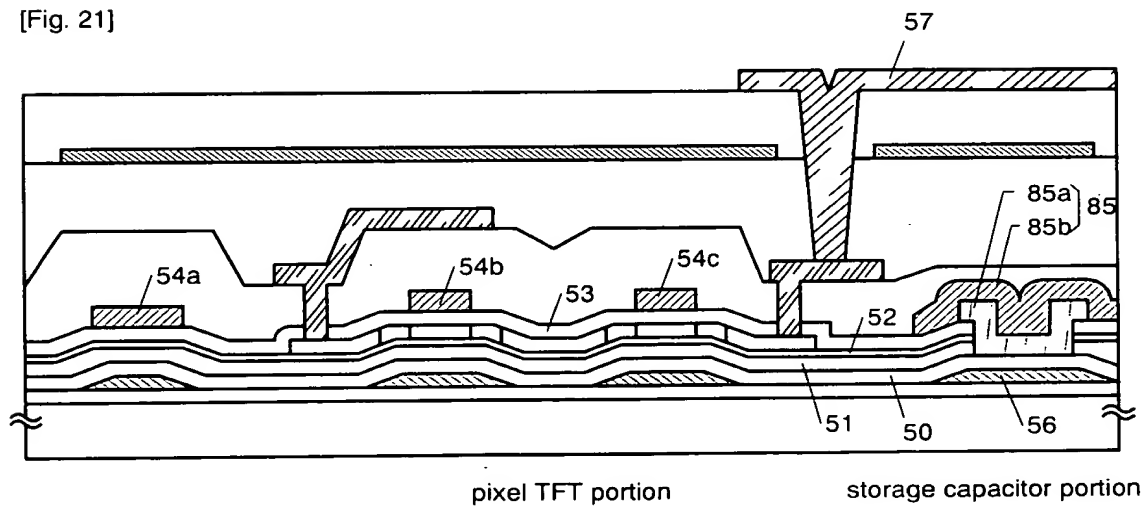
pixel TFT portion

storage capacitor portion

[Fig. 20]



[Fig. 21]



[illegible]